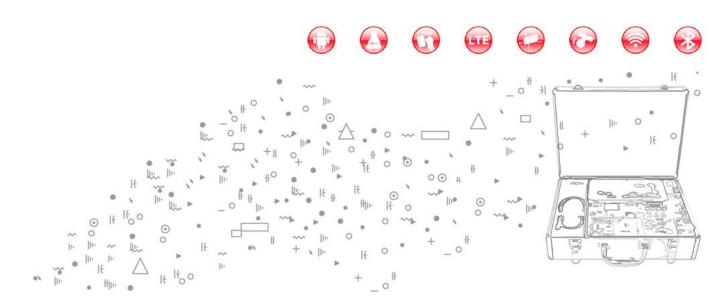
Embedded System

1. Introduction



CONTENTS

- 1. Embedded System
- 2. Real Time System
- 3. Embedded OS
- 4. Embedded System Application
- 5. Processor
- 6. CISC Vs RISC
- 7. ARM RISC
- 8. Application Processor (AP)
- 9. Multicore Processor
- 10. Appendix

1. Embedded System

- "Embedded"
- Embedded System → Electronic Control System containing Computer Hardware & Software
- Contemporary ES → Special Computer Unit with Microprocessor or Microcontroller for achieving special purposes
- PC → General purpose, Not an ES!
- A computer system with special purposes → ES → Various Applications

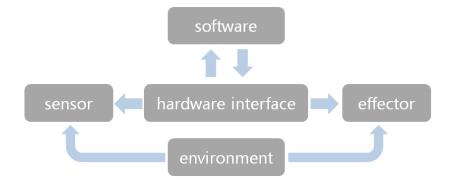
1. Embedded System

• Example of ES



2. Real Time system

- In general, ES responses or treating with user's input or environments' changes
- General ES → Exact Operation of Logically Defined Functions with the predefined sequences
- RT system → ES + "on-time / in-time"
- RT system
 - : The time of (Data Sensing + CPU handling + Actuator Handling) < the due date



3. Embedded OS

- Early ES → Designed only for achieving special objectives → The existence of OS was too much
- Recent ES → Network / Multimedia → Complex architectures → OS is needed!
- Recent ES = RT → RTOS is introduced into ES
- Current → ES' OS = RTOS

3. Embedded OS

Embedded OS → RTOS (Real Time OS)/ GPOS (General Purpose OS)

RTOS(Real Time OS)

- Generate output within the due date
- Not a fast processing, but JIT handling
- General RTOS considers: response speed, interrupt), Efficiency, Scalability, Portability

GPOS(General Purpose OS)

- GPOS = Windows NT, Windows 7/8/10, DOS, Linux, UNIX, Macintosh OS
- Needed Large Memory & ROM
- MMU (Memory Management Unit) is needed for handling Local File System, Paged Virtual Memory

Market of ES > Market of General PC



| Category | Contents | | | | |
|----------------|--|--|--|--|--|
| Car | Smart Car, Car Integrated Control System, Car-to-Car Communication | | | | |
| Vessel | Intelligent Vessel, e-navigation, Wireless Communication | | | | |
| Military | NX military communication, Air force S/W, Drone Network | | | | |
| Architect | U-city, EMP, Home network | | | | |
| Medical System | Surgery Robot, U-Health | | | | |

Information Terminal

- PDA, Mobile phone, Tablet
- RTOS → GPOS



Traffic and Vehicle

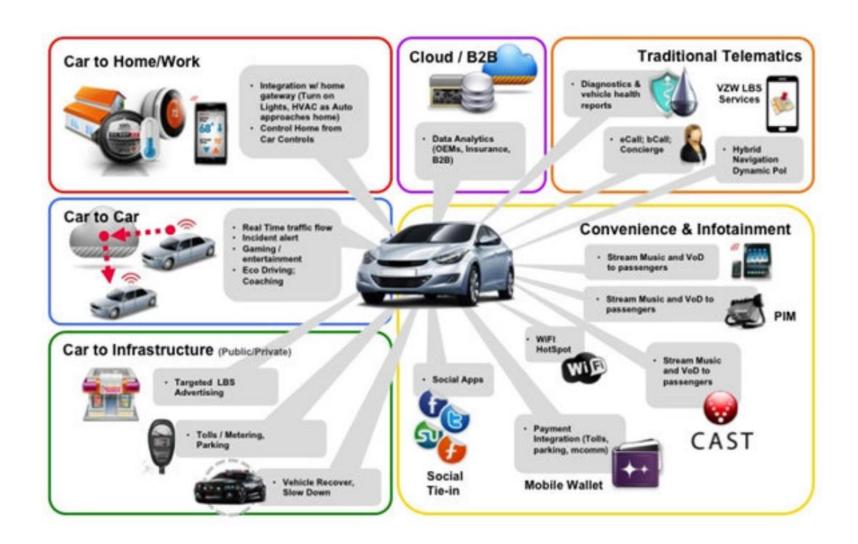
- Car + ICT Convergence
- LBS











https://en.wikipedia.org/wiki/Google driverless car

Did you know Google's self-driving cars can't handle 99% of roads in the US?



Credit: Google

Many people have heard that Google's autonomous cars can "drive anywhere a car can legally drive," but it can't drive in snow, heavy rains, see "unmapped" traffic lights or stop signs. In other words, Google's self-driving cars can handle the "matrix" but it can't navigate on 99% of the roads in the U.S.

MORE LIKE THIS

Google's driverless car is truly hands-off -- there's no steering wheel

100 self-driving Volvos to hit the streets of Sweden



Once your car's connected to the Internet, who guards your privacy?

on IDG Answers

How does Simply Secure improve cloud security?



SCM and Finance

• POS, RF TAG, ATM, ID Card



Information Entertainment / Appliance

ullet Smart TV ullet TV + OS ullet Internet, Game, POS, SNS + TV



Industry and Control

• FA(Factory Automation) & PLC(Programmable Logic Controller)

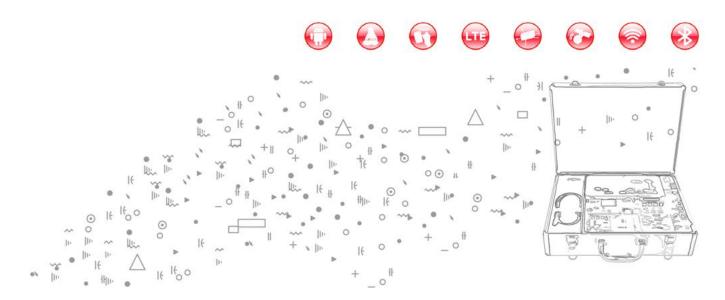


Medical Application

Virtual Solution, U-health



2. Embedded Processor



5. Processor

- The first ES development → What is the processor of ES ?
- Processor → CPU
- When the CPU is fixed, OS is selected. Then, ES is builted
- General Classification of Processor → With "Data bus Size" → 8, 16, 32, 64, 128 bit



CISC, RISC type Processors (Intel Vs. ARM)

6. CISC Vs. RISC

| Classification | CISC | RISC |
|--------------------|---|---|
| CPU instruction | Many Commands Various Length Many execution cycle | Fixed Length Size of Word = Size of Data bus The same execution cycle |
| Circuit | Complex | Simple |
| Memory Usage | Highly efficient | Low efficiency |
| Program | Short | Long |
| Compiler | Complicated | Comparatively Simple |
| Manufacturer | Intel, AMD, Atmel | SAMSUNG, TI, Atmel, ST |

CISC- Complex Instruction Set Computer RISC – Reduced Instruction Set Computer

7. ARM RISC

● ARM(Advanced RISC Machine) → RISC-based 32bit embedded processor

RISC

- load-store architecture
- fixed 32bit command
- address type

ARM RISC 기능

- 16 bit command is allowed
- Conditional command architecture
- optimal number of registers







Barrel Shift Register

- Barrel Shift is installed on ALU input layer→ Easy shift → Fast Execution
- Less Memory Usage, Cheaper, Low energy consumption

8. Application Processor (AP)

Application Processor

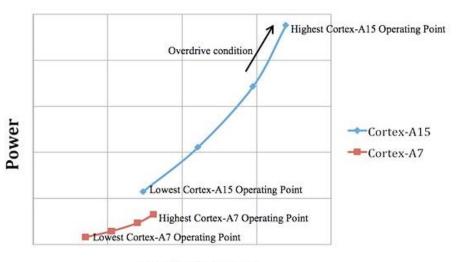
- Mobile Device's processor
- ullet Smart phone ullet Communication is important ullet Modem's processor (Subsidiary Processor) is important ullet It substitute the existing main processor → Application-specific processor → Application Processor
- AP → two trends → 1) Multimedia driven AP or 2) Performance/Speed driven AP
- Current Trends → Performance / Speed driven AP
- General Smart Phone AP → ARM architecture
- ARM 7/9/11 → Cortex
- 2013 → Cortex A9 architecture
- AP + Memory + Controller → one Chip → System on Chip → SoC
- 2015, 10 → Cortex architecture A57→ ARM v8-A



8. Application Processor (AP)

ARM Trends

- High resolution display, Powerful Multimedia, Low Energy Consumption
- Big Little Architecture"High Speed Core Set" + "Low Energy Core Set"





Highlights

- · 4X ARM Cortex A15 cores at 1.8GHz
- 4X ARM Cortez A7 cores at 1.2GHz
- 28nm Samsung manufacturing process
- Graphics: PowerVR SGX-544MP3 at 533MHz

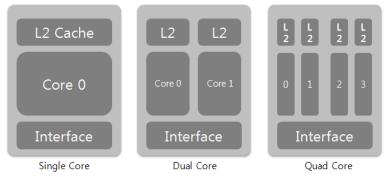
Performance

The first Big Little Architecture AP → Exynos5 Octa

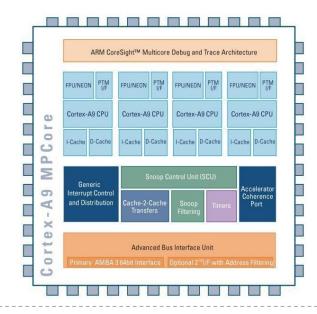
9. Multicore Processor

Current AP Trends → Multi cores

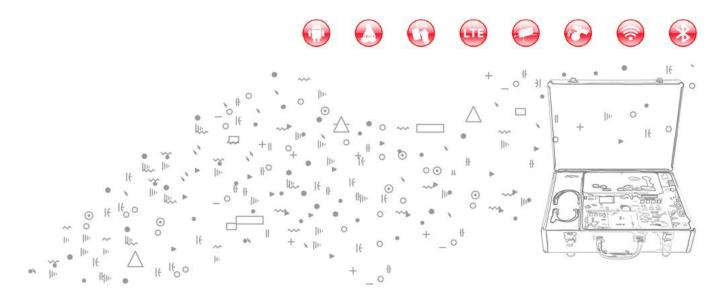
• Performance level up per a core < Multi core with common abilities cores



Cortex MpCore



Appendix



A. ARM Cortex-A9

| Туре | Architecture Ver. | Core | Function | Cache |
|-------|----------------------|----------------|--|-------------------------------|
| ARM11 | ARMv6 | ARM1136J(F)-S | SIMD, Jazelle DBX, (VFP) 8-stage Pipeline | variable, MMU |
| | ARMv6T2 | ARM1156T2(F)-S | SIMD, Thumb-2, (VFP) 9-stage Pipeline | variable, MPU |
| | ARMv6KZ | ARM1176JZ(F)-S | SIMD, Jazelle DBX, (VFP) | variable MMU+TrustZon e |
| | ARMv6K | ARM11 MPCore | 1-4 core SMP, SIMD Jazelle DBX, (VFP) | variable, MMU |

B. ARM Cortex-A9

| Туре | Architecture Ver. | Core | Function | Cache |
|--------|----------------------|---------------------|--|-------------------------------------|
| Cortex | ARMv7-A | Cortex-A8 | Application profile, VFP, NEON, Jazelle RCT, Th umb-2, 13-stage, perscalar pipeline | variable (L1+L2), MMU +TrustZone |
| | | Cortex-A9 | Application profile, (VFP), (NEON) Jazelle RCT and DBX, Thumb-2 Out-of-order speculative issue superscalar | MMU+TrustZone |
| | | Cortex-A9 MPCore | As Cortex-A9, 1-4 코어 SMP | MMU+TrustZone |
| | ARMv7-R | Cortex-R4(F) | Embedded profile, (FPU) | variable Cache MPU optional |
| | ARMv7-M | Cortex-M3 | Microcontroller profile, Thumb-2 only. | Cache, (MPU) |
| | ARMv6-M | Cortex-M1 | FPGA targeted, Micro controller profile | tightly coupled memory optional. |